## REMARKS

### *Drawings*

**The drawings are objected to under 37 CFR 1.83(a) because they fail to show the steps represented by blocks 402-408 as described in the specification.**

The Examiner has requested that the Applicant label the blocks in FIG. 4. Of course, the blocks are already labeled insofar as they contain reference numerals that refer to identifying and descriptive material in the specification. That the drawings lack a textual repetition of that material is principally due to the very large amount of that textual material, the inclusion of which is discouraged by USPTO practice and strongly disapproved by PCT practice, the United States being a PCT Treaty signatory. See, for example, 37 CFR §1.74 ("...the detailed description of the invention shall refer...to the different parts by use of reference letters or numerals (*preferably the latter*).") and PCT Rule 11.11 ("...drawings shall *not* contain text matter, except a single word or words, when *absolutely indispensable*...") (italics added for clarity). Additionally, inclusion of such extensive language is quite burdensome where international patent applications are associated and corresponding translated drawings are required. Finally, the protocol followed herein in FIG. 4 is already accepted and approved by the USPTO as shown, for example, by FIG. 2 of issued U.S. Patent No. 6,943,057 (not of record herein).

Accordingly, the Examiner is courteously and respectfully requested to withdraw the drawings request in view of the above explanations.

### *Claim Rejections - 35 USC §102*

**Claims 1-20 are rejected under 35 U.S.C. §102(e) as being anticipated by Stine et al. (U.S. Patent No. 6,901,564 B2, hereinafter "Stine").**

Stine provides a system and method for product yield prediction. The yield for a proposed integrated circuit design is predicted by processing a wafer to have a portion fabricated with at least one layout attribute of the proposed integrated circuit. The portion of the wafer is analyzed to determine an actual yield associated with the proposed layout attribute. A systematic yield associated with the proposed layout attribute is determined

based on the actual yield and a predicted yield associated with the proposed layout attribute. The predicted yield assumes that random defects are the only yield loss mechanism. A yield of an actual or proposed product layout is predicted for the integrated circuit based on the systematic yield.

### *Summary of Applicant's Arguments*

The present invention discloses and claims methods and systems for making real-time production lot decisions at intermediate stages in the fabrication of actual semiconductor devices. The present invention is not directed to designing semiconductor devices, nor to testing hypothetical layout configurations during the designing thereof. The present invention improves production decisions concerning whether or not to continue with the production of a given production lot of semiconductor devices, the fabrication of which is intended to be completed if it is determined by the present invention that completion of the production lot is commercially feasible.

Stine, on the other hand, has nothing to do with production lot completion decisions. The methods and systems of Stine are directed entirely to semiconductor design stages, not to semiconductor production. Stine provides for testing various proposed layout elements as a semiconductor device is being designed, not after it is in production. Stine never actually produces semiconductor devices in production lots, and never makes nor discloses anything concerning decisions about whether to continue or discontinue the further processing of a production lot.

The claims have accordingly been amended to make these distinctions more clear, and to make more clear that Stine thus fails to anticipate the present invention under 35 USC §102(e), as now claimed. For these reasons, the rejection should be withdrawn, the claims should be allowed, and the application should be passed to issuance.

### *Detailed Response to the Rejection*

Pursuant to claims 1 and 11, these independent claims have been clarified to amend the previously claimed combination, as exemplified in claim 1, to now include the limitations that:

"locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot to generate data concerning at least one defect in the semiconductor wafer at an intermediate processing stage;
...; and
...to determine the subsequent disposition of the wafer production lot."

The support for the above amendments is on page 7, lines 18–21; page 7, lines 23–26; page 7, line 32 through page 8, line 3; page 8, lines 5–6; page 8, line 21; and page 9, lines 16–18.

The Examiner states in the Office Action dated March 31, 2006:

> "(b) generating data concerning at least one defect in the semiconductor wafers at an intermediate stage (see col. 4, II. 41 - 59; col. 5, II. 40 - 51);...and (d) utilizing the layer model to determine the subsequent disposition of the wafer lot (see again Figs. 1 and 2; col. 3, line 65 - col. 4, line 40 which cite these elements)."

However, Stine does not disclose "locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot". Stine is concerned with pre-production design phases, and with testing alternative designs, not with making production lot decisions for a fixed-configuration design that is already in production. In fact, Stine does not even refer to, mention, or disclose wafer production lots, because Stine is not dealing with production decisions for a finalized production design configuration. Similarly, Stine does not refer to, mention, or disclose locating and defining current defects (i.e., actual defects) at an actual (as contrasted with Stine's experimental) intermediate processing stage of such a fixed-design wafer production lot, "to determine the subsequent disposition of the wafer production lot", as claimed. Stine's FIGs. 1 and 2, and Stine's specification, do not teach the claimed limitations, as explained in Stine's column 3, line 65, through column 4, line 59 (cited by the Examiner), and column 5, lines 40–51 (cited by the Examiner), which state:

> "Short flow is defined as encompassing only a specific subset of the total number of process steps in the integrated circuit fabrication cycle...a characterization vehicle such as one designed to investigate manufacturability
> ...
> The characterization vehicle 12 defines features which match one or more attributes of the proposed product layout. For example, the characterization vehicle 12 might define a short flow test vehicle having a partial layout which includes features which are representative of the proposed

product layout (e.g. examples of line size, spacing and periodicity; line bends and runs; etc.) in order to determine the maladies likely afflicting those specific design types and causing yield loss.

The characterization vehicle 12 might also define one or more active regions and neighboring features of the proposed design in order to explore impact of layout neighborhood on device performance and process parameters; model device parameters as a function of layout attributes; and determine which device correlate best with product performance. Furthermore, by constructing and analyzing a sufficient number of short flow vehicles such that the range of all possible or a major subset of all the modular components of the entire process is exercised, a full evaluation of many if not all of the yield problems which will afflict the specific product manufactured can be uncovered, modeled, and/or diagnosed.

In addition to providing information for assessing and diagnosing yield problems likely to be seen by the product(s) under manufacture, the characterization vehicle is designed to produce yield models 16 which can be used for accurate yield prediction. These yield models 16 can be used for purposes including, but not limited to, product planning, prioritizing yield improvement activities across the entire process, and modifying the original design of the product itself to make it more manufacturable.

...

The characterization vehicle 12 is preferably in the form of a GDS 2 layout on a tape or disc which is then used to produce a reticle set...defined by the characterization vehicle 12." (column 3, line 65, – column 4, line 59) [deletions and underlining for clarity]

"One type of characterization vehicle is a metal short flow characterization vehicle. The purpose of the metal short flow characterization vehicle is to quantify the printability and manufacturability of a single interconnect layer...Conducting short flow experiments using a metal short flow mask, enables experiments and analysis to be carried out in rapid succession to eliminate or minimize any systematic yield or random defect yield issue that is detected without having to wait for complete flow runs to finish." (column 5, lines 40–51) [deletions and underlining for clarity]

Thus Stine does not disclose locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot, locating and defining current defects at an actual intermediate processing stage of such a wafer production lot, and consequentially determining the subsequent disposition of the wafer production lot, as claimed in claims 1 and 11.

Based on the above, it is respectfully submitted that independent claims 1 and 11, and the respective claims 2–5 and 12–15 depending therefrom, are allowable under 35 USC §102(e) because:

> "Anticipation requires the disclosure in a single prior art reference disclosure of each and every element of the claim under consideration." W.L. Gore & Assocs. v. Garlock, Inc., 721 F.2d 1540, 220 USPQ 303, 313 (Fed. Cir. 1983) (citing Soundscriber Corp. v. United States, 360 F.2d 954, 960, 148 USPQ 298, 301 (Ct. Cl.), *adopted*, 149 USPQ 640 (Ct. Cl. 1966)), *cert. denied*, 469 U.S. 851 (1984). Carella v. Starlight Archery, 804 F.2d 135, 138, 231 USPQ 644, 646 (Fed. Cir.), *modified on reh'g*, 1 USPQ 2d 1209 (Fed. Cir. 1986); RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

Regarding claims 2 and 3, these dependent claims each depend from independent claim 1 and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 2 and 3 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claim 4, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof. Allowance of claim 4 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claim 5, this dependent claim depends from independent claim 1 and is believed to be allowable since it contains all the limitations set forth therein and additionally claims non-obvious combinations thereof. Allowance of claim 5 is therefore respectfully requested on this ground as well because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Referring to claims 6 and 16, these claims have been similarly amended as claims 1 and 11 to clarify that the combination of the present invention, as exemplified in claim 6, includes the limitations of:

> "locating and defining current defects in partially completed dies of semiconductor wafers in a wafer production lot to generate and extract data concerning defects in the semiconductor wafers at an intermediate processing stage;
> ...; and
> ...to determine the subsequent disposition of the wafer production lot."

The same issues have therefore been discussed in detail above with respect to the rejection of claims 1 and 11, and those arguments are equally applicable to the rejection of claims 6 and 16, showing that Stine does not disclose locating and defining current defects in partially completed dies of a semiconductor wafer in a wafer production lot, locating and defining current defects at an actual intermediate processing stage of such a wafer production lot, and consequentially determining the subsequent disposition of the wafer production lot, as claimed.

It is therefore respectfully submitted that independent claims 6 and 16, and the respective claims 7–10 and 17–20 depending therefrom, are allowable under 35 USC §102(e). Allowance of claims 6–10 and 16–20 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claims 7, 12, and 17, these dependent claims each depend from respective independent claims 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 7, 12, and 17 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claims 8, 13, and 18, these dependent claims each depend from respective independent claims 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 8, 13, and 18 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claims 9, 14, and 19, these dependent claims each depend from respective independent claims 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 9, 14, and 19 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

Regarding claims 10, 15, and 20, these dependent claims each depend from respective independent claims 6, 11, and 16, and are believed to be allowable since they contain all the

limitations set forth in the independent claim from which they depend and additionally claim non-obvious combinations thereof. Allowance of claims 10, 15, and 20 is therefore respectfully requested because of W.L. Gore & Assocs. v. Garlock, Inc. and the other cases cited therewith, *supra*.

***Conclusion***

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

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